IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group Art Unit: Unassigned Examiner: Unassigned

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| Applicant(s) | : | KUMAMOTO et al. |) |
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| Serial No. | : | Divisional of Appl. Serial No. 09/504,874 |) |
| Filed | : | January 30, 2004 |) INFORMATION) DISCLOSURE |
| For | : | SEMICONDUCTOR CHIP AND PRODUCTION PROCESS THEREFOR |))) |
| Attorney Ref | | AT 318 D1 |) |

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure, attached are copies of the Forms PTO-892 from the parent application, serial number, **09/504,874**, which the Examiner may wish to consult during examination of this Divisional Application thereof.

Respectfully submitted,

January 30, 2004 Date

Steven M. Rabin (Reg. No. 29.102)

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Notice of References Cited

Applicant/Patent
Kumamoto et al

Examiner
NItin Parekh

Application/Control No.
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Page 1 of 1

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¹ Dates in MM-YYYY format are publication dates.

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